ABSTRACT OF THE DISCLOSURE

A clock monitoring apparatus according to the invention including a main clock monitoring portion including a first counter for counting a main clock, issuing a normal operation confirming flag indicating that a normal operation is being carried out when the first counter is overflowed or reaches a previously determined set value, monitoring the normal operation confirming flag by a sub clock, issuing a first main clock stop flag having an output in correspondence with H (high level) / L (low level) of the normal operation confirming flag and a main clock initializing signal for initializing the main clock when the main clock is determined to stop and resetting the first main clock stop flag when the main clock is recovered by receiving the main clock initializing signal, and a sub clock switching control portion including a second counter for counting a signal output produced by calculating a logical sum of the sub clock and the first main clock stop flag at fall of the sub clock at a time point of generating the first main clock stop flag, switching to a sub clock operation by issuing a sub clock switching signal when the second counter output is overflowed or reaches a previously determined set value and resetting the second counter output when the main clock is recovered and a second main clock stop flag produced by inverting the first main clock stop flag and delaying the sub clock by a predetermined period by a main clock monitoring portion, is reset.